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FAIRCHILD SEMICONDUCTOR™

October 1987
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MM74C48
BCD-to-7 Segment Decoder

General Description

The MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test-blanking input/ripple-blanking output, and ripple-blanking inputs.

Features

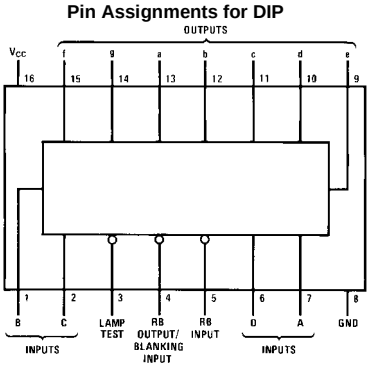
- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

Ordering Code:

Order Number	Package Number	Package Description
MM74C48N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

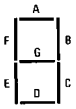
Connection Diagrams

Pin Assignments for DIP

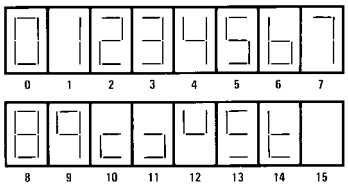


Top View

Segment Identification



Numerical Designations and Resultant Displays



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Truth Table

Decimal or Function	Inputs						BI/RBO (Note 1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	(Note 2)
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	(Note 2)
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(Note 3)
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(Note 4)
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(Note 5)

H = HIGH Level
L = LOW Level
X = Irrelevant

Note 1: One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 2: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be HIGH, if blanking of a decimal zero is not desired.

Note 3: When a LOW logic level is applied directly to the blanking input (BI), all segment outputs are LOW regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a LOW level with the lamp-test input HIGH, all segment outputs go LOW and the ripple-blanking output (RBO) goes to a LOW level (response condition).

Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open and a LOW is applied to the lamp-test input, all segment outputs are HIGH.

Absolute Maximum Ratings (Note 6)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 6: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
	(RB Output Only)	V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −50 μA	2.4			V
	(RB Output Only)					
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current	V_{CC} = 4.75V, V_{OUT} = 0.4V			−0.80	mA
	(P-Channel) (RB Output Only)	V_{CC} = 10V, V_{OUT} = 0.5V			−4.0	mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, V_{OUT} = V_{CC}	1.75	3.6		mA
	(N-Channel)	T_A = 25°C				
I_{SINK}	Output Sink Current	V_{CC} = 10V, V_{OUT} = V_{CC}	8.0	16		mA
	(N-Channel)	T_A = 25°C				
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, V_{OUT} = 3.4V	−20	−50		mA
	(NPN Bipolar)	V_{CC} = 5.0V, V_{OUT} = 3.0V		−65		mA
		V_{CC} = 10V, V_{OUT} = 8.4V	−20	−50		mA
		V_{CC} = 10V, V_{OUT} = 8.0V		−65		mA

AC Electrical Characteristics (Note 7)

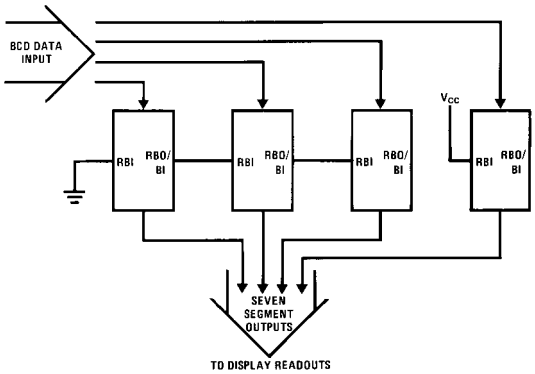
$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay to a "1" or "0" on	$V_{CC} = 5.0V$		450	1500	ns
	Segment Outputs from Data Inputs	$V_{CC} = 10V$		160	500	ns
t_{pd0}	Propagation Delay to a "0" on	$V_{CC} = 5.0V$		500	1600	ns
	Segment Outputs from RB Input	$V_{CC} = 10V$		180	550	ns
t_{pd0}	Propagation Delay to a "0" on	$V_{CC} = 5.0V$		350	1200	ns
	Segment Outputs from Blanking Input	$V_{CC} = 10V$		140	450	ns
t_{pd1}	Propagation Delay to a "1" on	$V_{CC} = 5.0V$		450	1500	ns
	Segment Outputs from Lamp Test	$V_{CC} = 10V$		160	500	ns
t_{pd1}	Propagation Delay to a "1" on RB	$V_{CC} = 5.0V$		600	2000	ns
	Output from RB Input	$V_{CC} = 10V$		250	800	ns
t_{pd0}	Propagation Delay to a "0" on RB	$V_{CC} = 5.0V$		140	450	ns
	Output from RB Input	$V_{CC} = 10V$		50	150	ns

Note 7: AC Parameters are guaranteed by DC correlated testing.

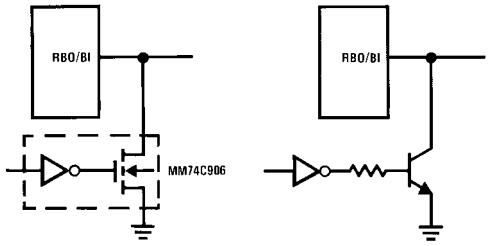
Typical Applications

Typical Connection Utilizing the Ripple-Blanking Feature



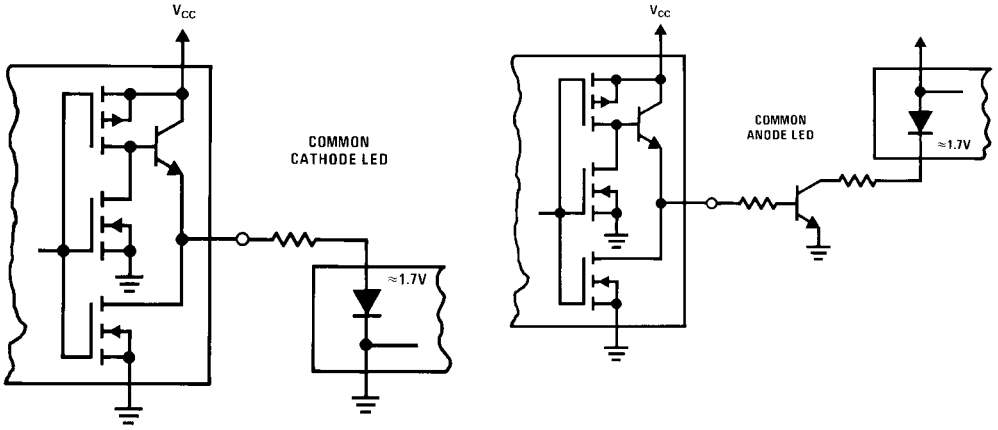
First three stages will blank leading zeros, the fourth stage will not blank zeros.

Blanking Input Connection Diagram

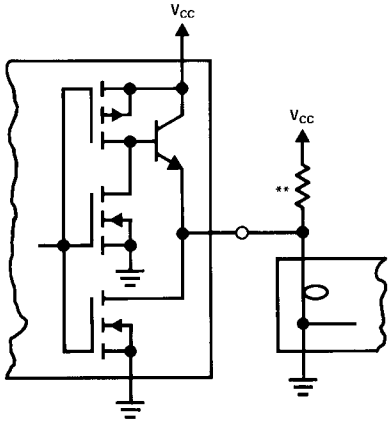


When RBO/BI is forced LOW, all segment outputs are off regardless of the state of any other input condition.

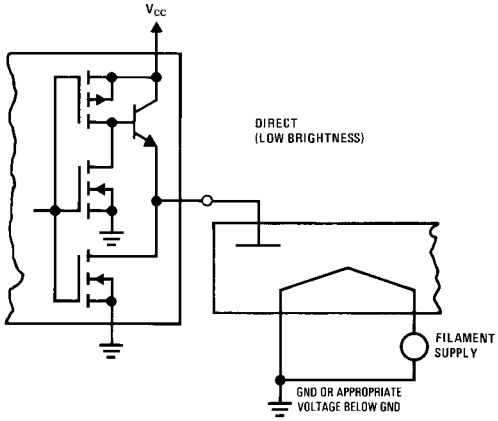
Light Emitting Diode (LED) Readout



Incandescent Readout

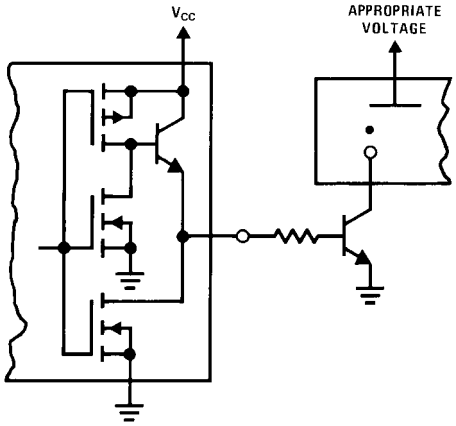


Fluorescent Readout

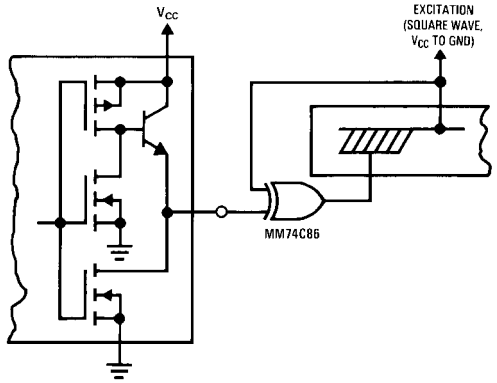


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Gas Discharge Readout

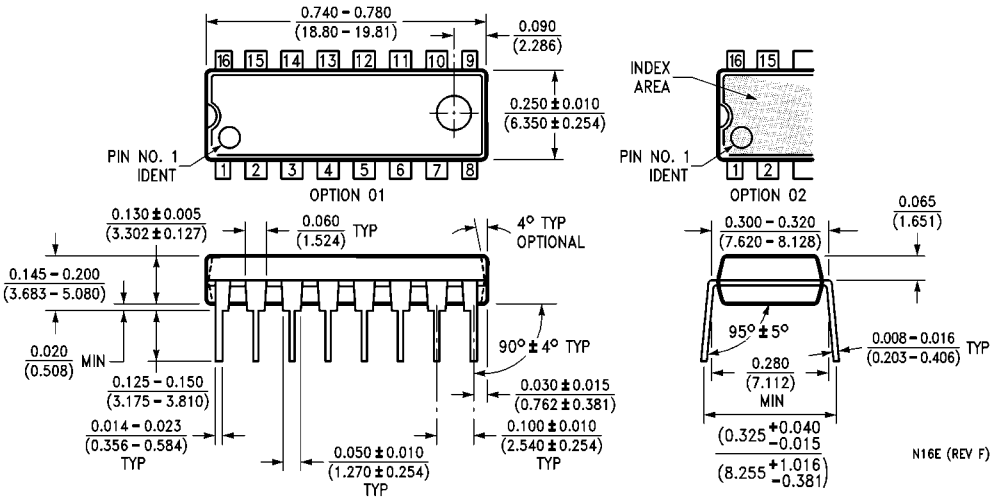


Liquid Crystal (LC) Readout



Direct DC drive of LC's not recommended for life of LC readouts.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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